**ÜS-PAT-NO**: 5817571

**DOCUMENT-IDENTIFIER:** US 5817571 A

TITLE: Multilayer interlevel dielectrics using phosphorus-doped glass

# Abstract Text - ABTX (1):

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A method for forming a planarized interlevel dielectric layer without degradation due to microloading effect is described. A first conformal layer of silicon dioxide is deposited overlying a conducting layer over an insulating layer on a semiconductor substrate. A second silicon dioxide layer is deposited overlying the first conformal silicon dioxide layer. A doped glass layer is deposited overlying the second silicon dioxide layer. The doped glass layer is coated with a spin-on-glass layer. The spin-on-glass layer is etched back until the interlevel dielectric layer is planarized. The microloading effects from the etching back of the spin-on-glass layer of the interlevel dielectric layer are lower than microloading effects in a conventional interlevel dielectric layer.

## **Brief Summary Text - BSTX (6):**

However, when the silicon oxide layer 18 is exposed to CF.sub.4 /CHF.sub.3 plasma during etchback, oxygen atoms will be released from their Si--O bondings. These oxygen atoms consume the adjacent spin-on-glass Si--O bondings, thus enhancing the spin-on-glass etch rate. This is called the microloading effect. The etch recipe is tuned so that the silicon oxide and the spin-on-glass will be etched at the same rate. If microloading effects occur, the spin-on-glass etch rate is faster than expected; therefore more of. The spin-on-glass is consumed than expected. This results in degradation of the planarization.

#### **Brief Summary Text - BSTX (13):**

In accordance with the objects of the invention, a method for forming a planarized interlevel dielectric layer without degradation due to microloading effect is achieved. A first conformal layer of silicon dioxide is deposited overlying a conducting layer over an insulating layer on a semiconductor substrate. A second silicon dioxide layer is deposited overlying the first conformal silicon dioxide layer. A doped glass layer is deposited overlying the second silicon dioxide layer. The doped glass layer is coated with a spin-on-glass layer. The spin-on-glass layer is etched back until the interlevel dielectric layer is planarized. The microloading effects from the etching back of the spin-on-glass layer of the interlevel dielectric layer are lower than microloading effects in a conventional interlevel dielectric layer.

## **Detailed Description Text - DETX (10):**

The process of the invention significantly reduces the <u>microloading</u> effect after spin-on-<u>glass etchback</u> resulting in excellent planarization of the interlevel <u>dielectric</u> layer. It is believed that the mechanism of the reduction of the microloading effect may be twofold. First, the increased plasma etch rate selectivity of the doped glass to the spin-on-glass results in good planarization when the doped glass, such as PSG, and the spin-on-glass are exposed to plasma simultaneously. Secondly, fewer oxygen radicals are generated from the etched doped

glass capping layer 22 resulting in less of an enhanced spin-on-glass etch rate. In doped glass, oxygen is easily bonded to the dopant which may deactivate the oxygen atom reaction.

## **Detailed Description Text - DETX (11):**

Although any dopant can be added to the <u>glass</u> layer 22 to reduce the <u>microloading</u> effect, phosphorus is preferred in the process of the invention because phosphorus acts as a movement barrier to mobile charges resulting from plasma <u>etching</u>. Mobile charges come from the ambient and from photoresist and decrease the oxide dielectric properties, such as capacitance. A phosphosilicate glass (PSG) can prevent the penetration of mobile charges.

### **Detailed Description Text - DETX (13):**

The process of the invention results in excellent planarization of an intermetal <u>dielectric</u> layer with significantly reduced <u>microloading</u> effect at the spin-on<u>-glass etchback</u> step.

## Claims Text - CLTX (8):

etching back said spin-on-glass layer until said improved interlevel dielectric layer is planarized wherein microloading effects from said etching back of said spin-on-glass layer of said improved interlevel dielectric layer are lower than microloading effects in said conventional interlevel dielectric layer because of said directly underlying doped glass layer;

## Claims Text - CLTX (26):

etching back said spin-on-glass layer until said improved interlevel dielectric layer is planarized wherein microloading effects from said etching back of said spin-on-glass layer of said improved interlevel dielectric layer are lower than microloading effects in said conventional interlevel dielectric layer because of said TEOS-based doped glass layer underlying said spin-on-glass layer.

# Claims Text - CLTX (42):

etching back said spin-on-glass layer until said improved interlevel dielectric layer is planarized wherein microloading effects from said etching back of said spin-on-glass layer of said improved interlevel dielectric layer are lower than microloading effects in said conventional interlevel dielectric layer because of said doped glass layer underlying said spin-on-glass layer.